List of Publications

PEER-REVIEWED JOURNALS :

1. Anirban Sengupta, **Deepak Kachave**, "Spatial and Temporal Redundancy for Transient Fault Tolerant Datapath," in ***IEEE Transactions on Aerospace and Electronic Systems (TAES)***, vol. 54, no. 3, pp. 1168-1183, June 2018. **(Impact factor ~2)**
2. Anirban Sengupta, **Deepak Kachave**, Dipanjan Roy "Low Cost Functional Obfuscation of Reusable IP Cores used in CE Hardware through Robust Locking", ***IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD)***, Accepted, March, 2018. **(Impact factor ~2)**
3. **Deepak Kachave**, Anirban Sengupta, "Fault Tolerant DSP core datapath against Omni-directional spatial impact of SET", in IEEE Canadian Journal of Electrical and Computer Engineering, Accepted February 2019 **(Impact factor ~1.0)**
4. **Deepak Kachave**, Anirban Sengupta, "Shielding CE Hardware Against Reverse-Engineering Attacks Through Functional Locking", in ***IEEE Consumer Electronics***, vol. 7, no. 2, pp. 111-114, March 2018. **(Impact factor ~1.5)**
5. **Deepak Kachave**, Anirban Sengupta, "Performance Degradation of DSP Cores due to NBTI Stress Attack (Invited Paper)", ***IEEE Potentials***, 2018.
6. **Deepak Kachave**, Anirban Sengupta, "Applying digital forensic for hardware protection : resolving false claim of IP ownership", ***IEEE VLSI Circuits & Systems Letter***, Volume 4, Issue 1, pp. 10 - 13, Feb 2018.
7. **Deepak Kachave**, Anirban Sengupta, Shubha Neema, Panugothu Sri Harsha " Effect of NBTI Stress on DSP cores used in CE Devices: Threat Model and Performance Estimation", ***IET Journal on Computers & Digital Techniques (CDT)***, Volume 12, Issue 6, pp. 268-278, 2018. **(Impact factor ~0.6)**
8. Anirban Sengupta, **Deepak Kachave** "Particle Swarm Optimisation Driven Low Cost Single Event Transient Fault Secured Design during Architectural Synthesis (Invited Paper)", ***IET Journal of Engineering***, p. 184-194, 2017
9. Anirban Sengupta, **Deepak Kachave** "Low Cost Fault Tolerance against kc-cycle and km-unit Transient for Loop Based Control Data Flow Graphs during Physically Aware High Level Synthesis", ***Elsevier Journal on Microelectronics Reliability***, Volume 74, July 2017, pp. 88-99. **(Impact factor ~1.2)**
10. Anirban Sengupta, **Deepak Kachave** "Forensic Engineering for Resolving Ownership Problem of Reusable IP Core generated during High Level Synthesis", ***Elsevier Journal on Future Generation Computer Systems***, Volume 80, Pages 29-46, March 2018. **(Impact factor ~4.6)**
11. **Deepak Kachave**, Anirban Sengupta, "Integrating Physical Level Design and High Level Synthesis for Simultaneous Multi-Cycle Transient and Multiple Transient Fault Resiliency of Application Specific Datapath Processors", ***Elsevier Journal on Microelectronics Reliability,*** Volume 60, Pages 141-152, May 2016. **(Impact factor ~1.2)**

BOOK CHAPTER :

1. Deepak Kachave, Anirban Sengupta, "Hardware Reliability Analysis of DSP Cores", ***IET Book: VLSI and Post-CMOS Devices, Circuits and Modelling***, Invited Book Chapter, 2017.

PEER-REVIEWED CONFERENCES :

1. Anirban Sengupta, Deepak Kachave, "Generating Multi-cycle and Multiple Transient Fault Resilient Design During Physically Aware High Level Synthesis," ***2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)***, Pittsburgh, PA, 2016, pp. 75-80.
2. Deepak Kachave, Anirban Sengupta, "Protecting Ownership of Reusable IP Core Generated during High Level Synthesis," ***2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)***, Gwalior, 2016, pp. 80-82.

3. Anirban Sengupta, Deepak Kachave, Shubha Neema, Panugothu Sri Harsha, "Reliability and Threat Analysis of NBTI Stress on DSP Cores," ***2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)***, Bhopal, 2017, pp. 11-14.
4. Anirban Sengupta, Deepak Kachave, "Integrating Compiler Driven Transformation and Simulated Annealing based Floorplan for Optimized Transient Fault Tolerant DSP cores," ***2018 IEEE International Symposium on Smart Electronic Systems (iSES)***, Hyderabad, 2018, (accepted and presented).