Supplementary Information

Multilevel Nanophotonic Resistive Switching in Ag-ITO-SiO_2 on Silicon with Enhanced Optical Storage Density

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I: Device Fabrication Method

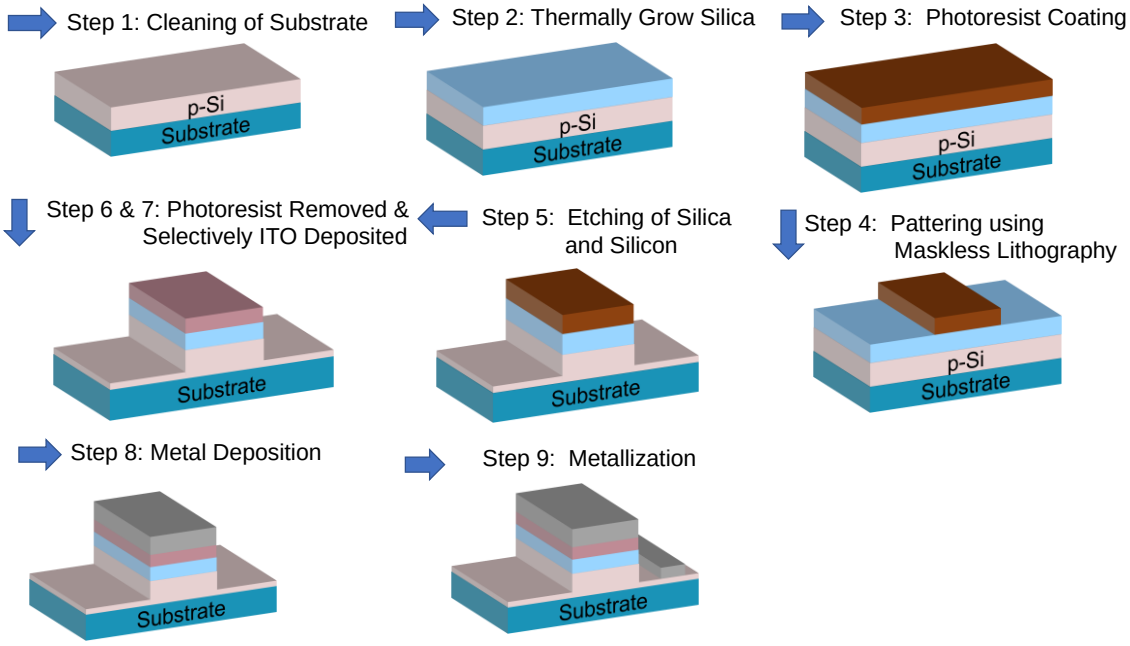

Fig. S1. 3D-schematic illustrates the standard CMOS-compatible fabrication process of the proposed engineered multilevel hybrid plasmonic waveguide on a p-type SOI wafer. The process involves sequential cleaning steps, thermal treatment of silica, photoresist coating, lithography patterning, wet etching of silicon and silica, removal of photoresist, deposition of ITO using RF sputtering, metal deposition via DC sputtering, and completion of metallization.

As illustrated in Fig. S1, a 3D schematic of the standard CMOS-compatible fabrication process for the proposed engineered device on a p-type SOI wafer. Initially, the wafer is cleaned sequentially with isopropyl alcohol (IPA), acetone, and deionized water. Subsequently, silica is thermally treated at 1000°C for 12 minutes in the presence of oxygen to serve as a protective layer during the wet etching of Si and as part of the active structure for the proposed device. Moving to the next step, photoresist (PR) coating is applied above the silica, followed by patterning is achieved through optical maskless lithography, and developing the samples. Tetramethylammonium hydroxide and diluted hydrofluoric acid are used, respectively, to etch p-Si and silica. Following the etching process, coated PR is removed, and the deposition of ITO is performed using RF sputtering in the selected area. Metal deposition is carried out by DC sputtering in the designated region, and finally, metallization is completed.

II: OPTOELECTRONIC MEASUREMENT SET UP

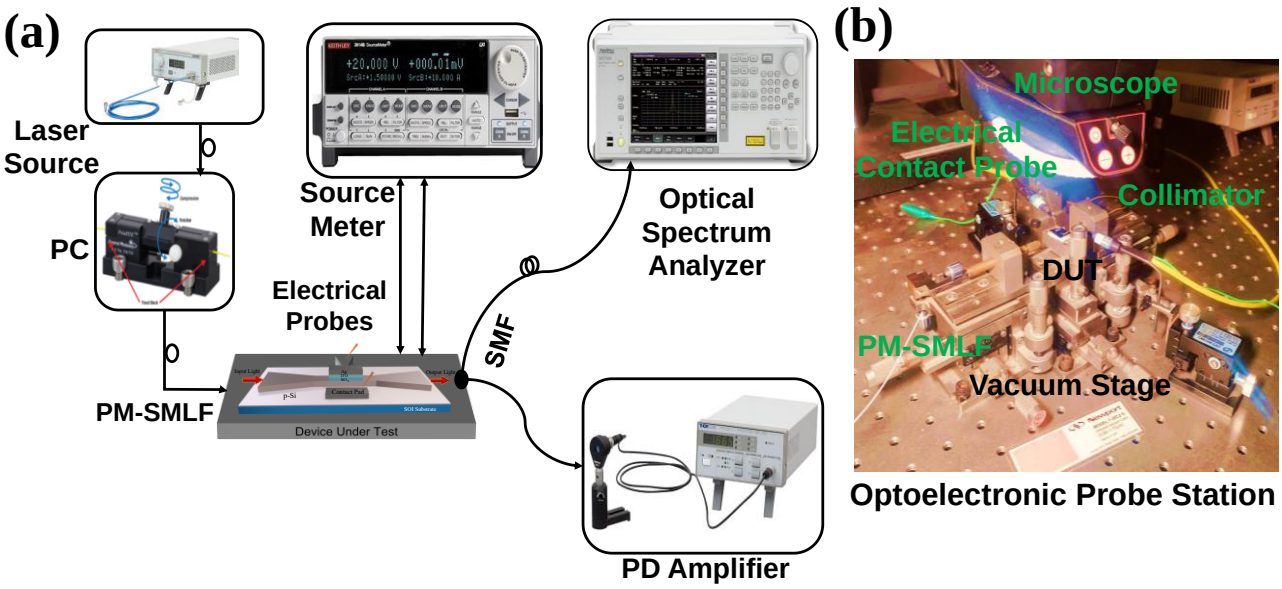

Fig. S2. Experimental optoelectronic characterization setup. (a) A schematic representation of setup comprising a laser source, polarization controller, tapered-lens PM SMF, optoelectronic probe station with the device under test (DUT), vacuum stage, microscope, source meter, OSA, and photodiode amplifier. The 1.55 μm wavelenth laser source has been used for read the multiple optical states. (b) Image of DUT on the optoelectronic probe station.

Figure S2 illustrates a schematic representation of the experimental optoelectronic characterization setup, including a laser source (LS, Thorlabs, Model No: S3FC-1550), polarization controller (Newport), polarization-maintaining (PM) tapered lensed single-mode fiber (SMF), vacuum stage, device under test (DUT), source meter (SM, Keithley, Model No: 2614B), optical microscope, optical-spectrum-analyzer (OSA, Anritsu, Model No: MS9740A-009), and photodiode (PD) amplifier (Thorlabs, Model No: PDA 200C). The DUT is positioned above the vacuum stage on the optoelectronic probe station. The PM tapered-lens fiber facilitates light coupling (TM polarized light) from the LS to the nanophotonic device, and the output light is collected through the collimator for analysis at the PD amplifier and OSA. Additionally, the multilevel nanophotonic device employs probe arms to establish connections with an electrical power supply. The DUT is shown in Fig. S2(b) which contain probe station, vacuum stage, PM tapered lensed SMF, collimator, and microscope.

III: Device Design and Mode Profile Confinement

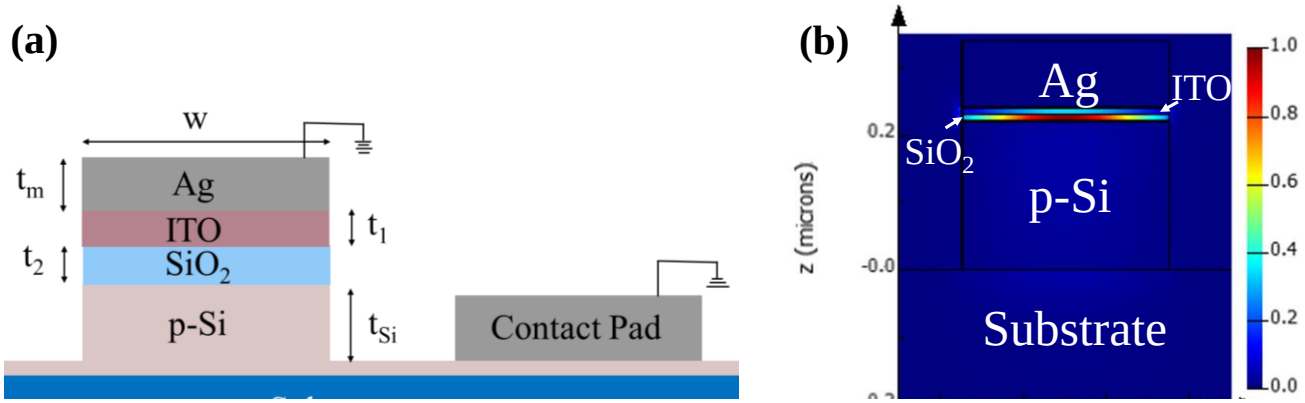

Fig. S3. (a) Cross-sectional view of the engineeried multilevel nanophotonic resistive switch and (b) Corresponding mode profile distribution at the telecommunication wavelength of 1.55 µm. Here, the thickness of the Ag, ITO, SiO_2 and Si has been considered as respectively, t_m, t_1, t_2, t_{Si}. The widths of the device is consider as w.